GX8002 Datasheet

Ultra-low-power voice processor

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1. Features

GX8002 is a ultra-low-power voice recognition and processing chip. It integrates NationalChip's ultra-low-power NPU(Neural Process Unit), 32-bit RISC MCU, hardware VAD(Voice activation detection) and rich interfaces. It can recognize voice keywords or voiceprint in ultra-low power. And it has package with small foot print and is easy to use or combined with other host processors.

MCU:

- 32-bit low-power RISC CPU with I/D cache and FPU
- Maximum frequency 50MHz

NPU:

- NationalChip's ultra-low-power and high-efficient neural processor, gxNPU V200
- Supports popular models such as DNN / CNN / LSTM

VAD:

- Hardware voice activity detection, can detect human voice by spectrum information from ambient noises

Memory:

- Built-in SRAM, size 208KB
- SIP Nor Flash, size 256KB or 512KB

Audio ADC:

- Low-power audio ADC with SNR 65dB and DR 65dB
- Programmable gain amplifier, supports 20~50dB gain with 1dB per step

Audio interfaces:

- Dual-channel PDM interface, supports master and slave mode
- One I2S input with TDM mode support
- Two I2S output interface, master/ slave configurable
- Dual-channel Audio DAC output

Communication interfaces:

- Two UARTs
- I2C Master and Salve
- SPI Master /Slave configurable
- GPIOs

System control:

- Integrates POR(power on reset)
- Internal 32KHz, 24MHz OSC
- Supports external 32KHz crystal

Voltage supply:

- Supports 1.8v or 3.3v IO power
- Integrates LDO for core power
- Supports 0.85v ~ 3.3v core power input

Typical power consumption:

- VAD Standby: < 100uW
- Wake-up: < 1mW
- Average power: < 300uW

Note: power measured in 25 degree

Package Type:

QFN20, 3mm x 3mm

2. Chip Architecture

2.1. Block Diagram

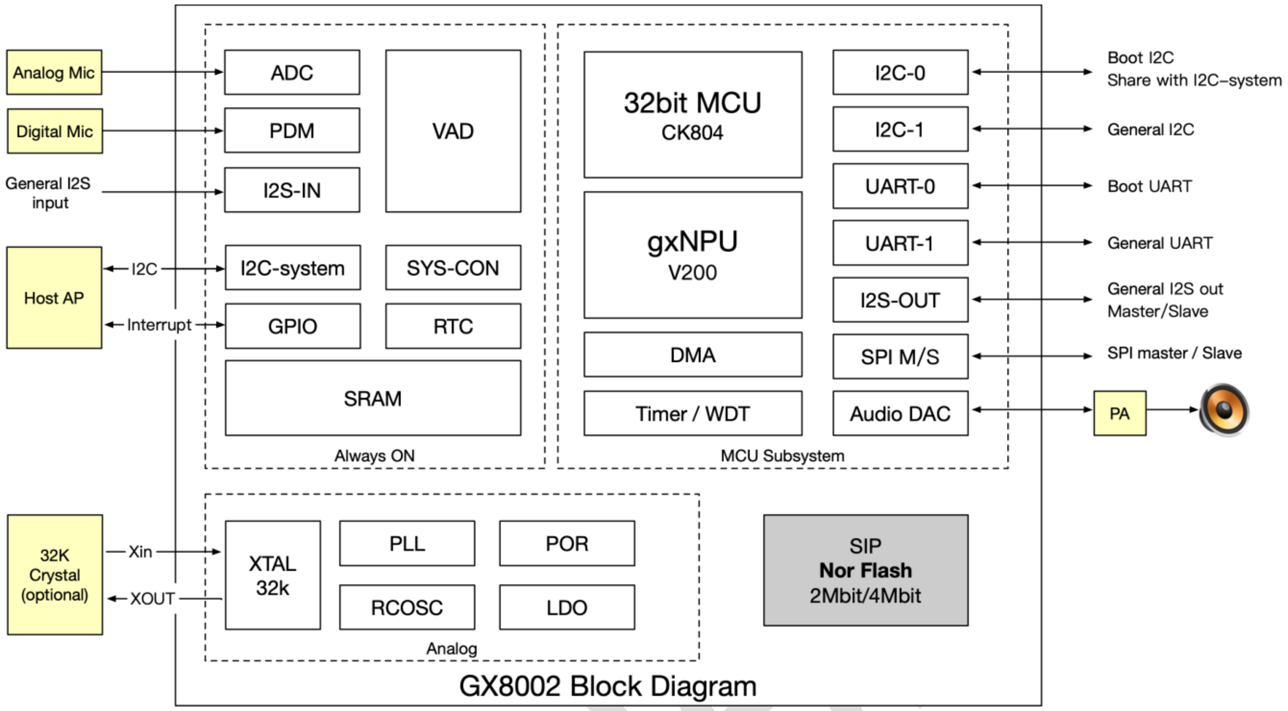


Figure 2-1 GX8002 chip block diagram

The GX8002 chipset can be divided into four parts: the first part is an Always On domain that consists of the voice input, VAD detection and system control modules, the second part is the MCU subsystem, the third part is the analog subsystem, and the last part is a SIP packaged Nor Flash with the size of 256KB or 512KB. MCU subsystem can be powered off to reduce power consumption. And in sleep mode, VAD, GPIO, RTC interrupts can be used to wake up the whole system.

3. Pin Description

3.1. Pin Map

The GX8002 is available in 20-pin QFN20(3x3) package with EPAD.

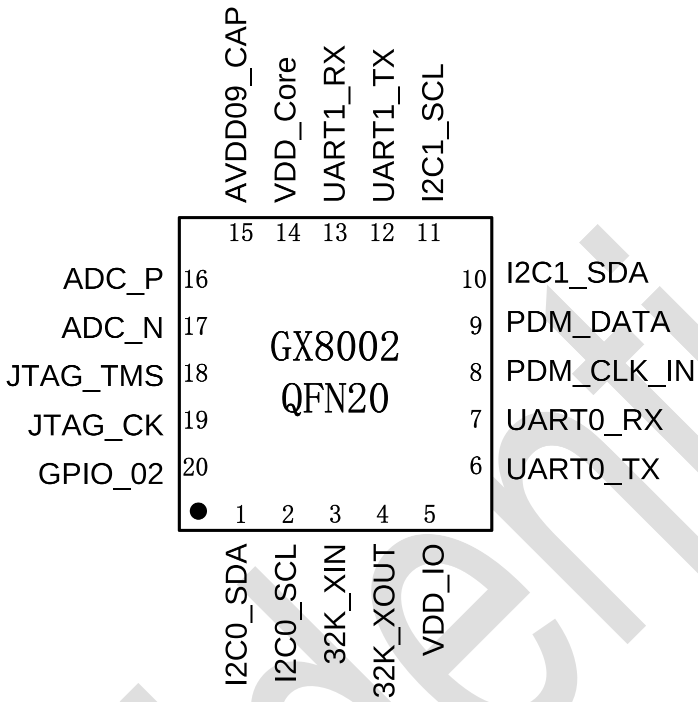


Figure 3-1 GX8002 pin map

3.2. Acronyms

DP => Digital Power

AP => Analog Power

I => Digital Input

O => Digital Output

IO => Digital Bi-directional

OD => Open Drive

AI => Analog Input

AO => Analog Output

3.3. Pin Multiplexing Functions

Table 3-1 Pin mux

Pin	Function00	Function01	Function02	Function03	Function04	Function05	Function06	Function07	Fuction08	Fuction09	Fuction10	Fuction11	Fuction12
01	I2C0_SDA	GPIO_03	PDM_CLK_IN	PDM_CLK_OUT									
02	I2C0_SCL	GPIO_04	PDM_DATA										
06	UART0_TX	GPIO_05	I2C1_SDA	PDM_CLK_IN	DAC_OUT_L	PDM_CLK_OUT							
07	UART0_RX	GPIO_06	I2C1_SCL	PDM_DATA	DAC_OUT_R	EXT_CLK_IN							
08	PDM_CLK_IN	GPIO_07	I2S_IN_MCLK_OUT	I2S_OUT_MCLK_OUT	SPI_SCLK_M	SPI_SCLK_S	REC_MCLK_OUT	DAC_OUT_L	I2S_OUT_MCLK_IN	REC_MCLK_IN	I2S_IN_MCLK_IN	UART0_CTS	PDM_CLK_OUT
09	PDM_DATA	GPIO_08	I2S_IN_LRCLK_OUT	I2S_OUT_LRCLK_OUT	SPI_MOSI_M	SPI_MOSI_S	REC_LRCLK_OUT	DAC_OUT_R	I2S_OUT_LRCLK_IN	REC_LRCLK_IN	I2S_IN_LRCLK_IN	UART0_RTS	EXT_CLK_IN
10	I2C1_SDA	GPIO_09	I2S_IN_BCLK_OUT	I2S_OUT_BCLK_OUT	SPI_CSn_M	SPI_CSn_S	REC_BCLK_OUT	UART1_CTS	I2S_OUT_BCLK_IN	REC_BCLK_IN	I2S_IN_BCLK_IN		
11	I2C1_SCL	GPIO_10	I2S_IN_DATA_IN	I2S_OUT_DATA_OUT	SPI_MISO_M	SPI_MISO_S	REC_DATA_OUT	UART1_RTS	EXT_CLK_IN				
12	UART1_TX	GPIO_11	I2S_IN_MCLK_OUT	I2S_OUT_MCLK_OUT	SPI_SCLK_M	SPI_SCLK_S	REC_MCLK_OUT	DAC_OUT_L	I2S_OUT_MCLK_IN	REC_MCLK_IN	I2S_IN_MCLK_IN		
13	UART1_RX	GPIO_12	I2S_IN_LRCLK_OUT	I2S_OUT_LRCLK_OUT	SPI_MOSI_M	SPI_MOSI_S	REC_LRCLK_OUT	DAC_OUT_R	I2S_OUT_LRCLK_IN	REC_LRCLK_IN	I2S_IN_LRCLK_IN		
18	JTAG_TMS	GPIO_00	I2S_IN_BCLK_OUT	I2S_OUT_BCLK_OUT	SPI_CSn_M	SPI_CSn_S	REC_BCLK_OUT	PDM_DATA	I2S_OUT_BCLK_IN	REC_BCLK_IN	I2S_IN_BCLK_IN		
19	JTAG_CK	GPIO_01	I2S_IN_DATA_IN	I2S_OUT_DATA_OUT	SPI_MISO_M	SPI_MISO_S	REC_DATA_OUT	PDM_CLK_IN	EXT_CLK_IN	PDM_CLK_OUT			
20	GPIO_02	EXT_CLK_IN											

3.4. Power and Analog Pins

Table 3-2 Power and analog pins

Pin Number	Pin Name	Type	Description
5	VDD_IO	DP	Digital IO power, can be 1.8v/3.3v
14	VDD_CORE	DP	Digital and ADC core power, can be 0.9v~3.3v
15	AVDD_CAP	AP	Connect to capacitor for analog power
16	ADC_P	AI	Audio ADC input, P port
17	ADC_N	AI	Audio ADC input, N port

3.5. System Clock Pins

Table 3-3 System operation pins

Pin Number	Pin Name	Type	Description
3	XIN	I	32KHz crystal input
4	XOUT	O	32KHz crystal output

3.6. Multi-function Pins

Table 3-4 Multi-function pins

PIN Number	PIN Name	I/O (Default)	PULL	Function Number	Function Name	Type	Description
1	I2C0_SDA	I	UP	0	I2C0_SDA	IO(OD)	Data of I2C0（Slave)
				1	GPIO_03	IO	General-purpose I/O
				2	PDM_CLK_IN	I	Clk of audio in pdm interface(slave)
				3	PDM_CLK_OUT	O	Clk of audio in pdm interface(Master)
2	I2C0_SCL	I	UP	0	I2C0_SCL	IO(OD)	Clk of I2C0（Slave)
				1	GPIO_04	IO	General-purpose I/O

PIN Number	PIN Name	I/O (Default)	PULL	Function Number	Function Name	Type	Description
				2	PDM_DATA	I	Data of audio in pdm interface
6	UART0_TX	O		0	UART0_TX	O	UART0 data transmit
				1	GPIO_05	IO	General-purpose I/O
				2	I2C1_SDA	IO(OD)	Data of I2C1（Master)
				3	PDM_CLK_IN	I	Clk of audio in pdm interface(Slave)
				4	DAC_OUT_L	O	Audio DAC left channel output
				5	PDM_CLK_OUT	O	Clk of audio in pdm interface(Master)
7	UART0_RX	I	UP	0	UART0_RX	I	UART0 data receive
				1	GPIO_06	IO	General-purpose I/O
				2	I2C1_SCL	IO(OD)	Clk of I2C1（Master)
				3	PDM_DATA	I	Dat of audio in pdm interface
				4	DAC_OUT_R	O	Audio DAC right channel output
				5	EXT_CLK_IN	I	External system clock input
8	PDM_CLK_IN	I	UP	0	PDM_CLK_IN	I	Clk of audio in pdm interface(Slave)
				1	GPIO_07	IO	General-purpose I/O
				2	I2S_IN_MCLK_OUT	O	MCLK of audio in i2s interface(Master)
				3	I2S_OUT_MCLK_OUT	O	MCLK of audio out i2s interface(Master)
				4	SPI_SCLK_M	O	SCK of SPI interface(Master)
				5	SPI_SCLK_S	I	SCK of SPI interface(Slave)
				6	REC_MCLK_OUT	O	Audio record PCM CLK out
				7	DAC_OUT_L	O	Audio DAC left channel output
				8	I2S_OUT_MCLK_IN	I	MCLK of audio out i2s interface(Slave)
				9	REC_MCLK_IN	I	Audio record PCM CLK in
				10	I2S_IN_MCLK_IN	I	MCLK of audio in i2s interface(Slave)
				11	UART0_CTS	I	CTS of UART0
				12	PDM_CLK_OUT	O	Clk of audio in pdm interface(Master)
9	PDM_DATA	I	UP	0	PDM_DATA	I	Dat of audio in pdm interface
				1	GPIO_08	IO	General-purpose I/O

PIN Number	PIN Name	I/O (Default)	PULL	Function Number	Function Name	Type	Description
				2	I2S_IN_LRCLK_OUT	O	LRCLK of audio in i2s interface(Master)
				3	I2S_OUT_LRCLK_OUT	O	LRCLK of audio out i2s interface(Master)
				4	SPI_MOSI_M	IO	MOSI of SPI interface(Master)
				5	SPI_MOSI_S	I	MOSI of SPI interface(Slave)
				6	REC_LRCLK_OUT	O	Audio record PCM LRCLK out
				7	DAC_OUT_R	O	Audio DAC right channel output
				8	I2S_OUT_LRCLK_IN	I	LRCLK of audio out i2s interface(Slave)
				9	REC_LRCLK_IN	I	Audio record PCM LRCLK in
				10	I2S_IN_LRCLK_IN	I	LRCLK of audio in i2s interface(Slave)
				11	UART0_RTS	O(OD)	RTS of UART0
				12	EXT_CLK_IN	I	External system clock input
10	I2C1_SDA	I	UP	0	I2C1_SDA	IO(OD)	Data of I2C1（Master)
				1	GPIO_09	IO	General-purpose I/O
				2	I2S_IN_BCLK_OUT	O	BCLK of audio in i2s interface(Master)
				3	I2S_OUT_BCLK_OUT	O	BCLK of audio out i2s interface(Master)
				4	SPI_CSn_M	O	CSn of SPI interface(Master)
				5	SPI_CSn_S	I	CSn of SPI interface(Slave)
				6	REC_BCLK_OUT	O	Audio record PCM BCLK out
				7	UART1_CTS	I	CTS of UART1
				8	I2S_OUT_BCLK_IN	I	BCLK of audio out i2s interface(Slave)
				9	REC_BCLK_IN	I	Audio record PCM BCLK in
				10	I2S_IN_BCLK_IN	I	BCLK of audio in i2s interface(Slave)
11	I2C1_SCL	I	UP	0	I2C1_SCL	IO(OD)	Clk of I2C1（Master)
				1	GPIO_10	IO	General-purpose I/O
				2	I2S_IN_DATA_IN	I	DATA of audio in I2S interface
				3	I2S_OUT_DATA_OUT	O	DATA of audio out I2S interface
				4	SPI_MISO_M	I	MISO of SPI interface(Master)

PIN Number	PIN Name	I/O (Default)	PULL	Function Number	Function Name	Type	Description
				5	SPI_MISO_S	IO	MISO of SPI interface(Slave)
				6	REC_DATA_OUT	O	Audio record PCM SDAT out
				7	UART1_RTS	O(OD)	RTS of UART1
				8	EXT_CLK_IN	I	External system clock input
12	UART1_TX	O		0	UART1_TX	O	UART1 data transmit
				1	GPIO_11	IO	General-purpose I/O
				2	I2S_IN_MCLK_OUT	O	MCLK of audio in i2s interface(Master)
				3	I2S_OUT_MCLK_OUT	O	MCLK of audio out i2s interface(Master)
				4	SPI_SCLK_M	O	SCK of SPI interface(Master)
				5	SPI_SCLK_S	I	SCK of SPI interface(Slave)
				6	REC_MCLK_OUT	O	Audio record PCM MCLK out
				7	DAC_OUT_L	O	Audio DAC left channel output
				8	I2S_OUT_MCLK_IN	I	MCLK of audio out i2s interface(Slave)
				9	REC_MCLK_IN	I	Audio record PCM MCLK in
				10	I2S_IN_MCLK_IN	I	MCLK of audio in i2s interface(Slave)
13	UART1_RX	I	UP	0	UART1_RX	I	UART1 data receive
				1	GPIO_12	IO	General-purpose I/O
				2	I2S_IN_LRCLK_OUT	O	LRCLK of audio in i2s interface(Master)
				3	I2S_OUT_LRCLK_OUT	O	LRCLK of audio out i2s interface(Master)
				4	SPI_MOSI_M	IO	MOSI of SPI interface(Master)
				5	SPI_MOSI_S	I	MOSI of SPI interface(Slave)
				6	REC_LRCLK_OUT	O	Audio record PCM LRCLK out
				7	DAC_OUT_R	O	Audio DAC right channel output
				8	I2S_OUT_LRCLK_IN	I	LRCLK of audio out i2s interface(Slave)
				9	REC_LRCLK_IN	I	Audio record PCM LRCLK in
				10	I2S_IN_LRCLK_IN	I	LRCLK of audio in i2s interface(Slave)

PIN Number	PIN Name	I/O (Default)	PULL	Function Number	Function Name	Type	Description
18	JTAG_TMS	I	UP	0	JTAG_TMS	IO	MCU Debug interface mode select
				1	GPIO[00]	IO	General-purpose I/O
				2	I2S_IN_BCLK_OUT	O	BCLK of audio in i2s interface(Master)
				3	I2S_OUT_BCLK_OUT	O	BCLK of audio out i2s interface(Master)
				4	SPI_CSn_M	O	CSn of SPI interface(Master)
				5	SPI_CSn_S	I	CSn of SPI interface(Slave)
				6	REC_BCLK_OUT	O	Audio record PCM BCLK out
				7	PDM_DATA	I	Data of audio in pdm interface
				8	I2S_OUT_BCLK_IN	I	BCLK of audio out i2s interface(Slave)
				9	REC_BCLK_IN	I	Audio record PCM BCLK in
				10	I2S_IN_BCLK_IN	I	BCLK of audio in i2s interface(Slave)
19	JTAG_CK	I	UP	0	JTAG_CK	I	MCU Debug interface clock
				1	GPIO_01	IO	General-purpose I/O
				2	I2S_IN_DATA_IN	I	DATA of audio in I2S interface
				3	I2S_OUT_DATA_OUT	O	DATA of audio out I2S interface
				4	SPI_MISO_M	I	MISO of SPI interface(Master)
				5	SPI_MISO_S	IO	MISO of SPI interface(Slave)
				6	REC_DATA_OUT	O	Audio record PCM SDAT out
				7	PDM_CLK_IN	I	Clk of audio in pdm interface(Slave)
				8	EXT_CLK_IN	I	External system clock input
				9	PDM_CLK_OUT	O	Clk of audio in pdm interface(Master)
20	GPIO_02	I	UP	0	GPIO_02	IO	General-purpose I/O Select I2C address 0x35 or 0x36 through GPIO_02 pull down during boot period, default 0x35
				1	EXT_CLK_IN	I	External system clock input

4. Function Overview

4.1. CPU Architecture

- 32-bit RISC MCU CK804, frequency up to 50MHz
- Instruction cache 4KB， data cache 8KB
- Supports DSP and FPU acceleration unit
- 32 interrupt sources in total
  - Each interrupt source can be independently enabled
  - Unmasked interrupts can wake up the chip in sleep mode

4.2. Memory

- Integrates 208KB SRAM
- Internally encapsulates 256KB / 512KB SPI NOR flash in SIP style
  - Supports standard, dual or quad mode of SPI interface
  - Allow to execute code (XIP) directly from the flash
  - SPI clock frequency up to 25MHz

4.3. Clock

- On-chip 32KHz/24MHz oscillator circuit
- Support external 32.768KHz crystal input
- One phase-locked loops (PLL) with programmable multiplier up to 50MHz
- Functional-unit clock gating integrated to reduce power

4.4. NPU

- NationalChip's gxNPU V200, low-power optimized version of neural process unit
- Supports DNN/CNN/DS-CNN/LSTM/GRU and other popular models
- Supports 8-bit quantization, and weights compression
- Compiler supports direct conversion from Tensorflow

4.5. System Peripheral

- I2C
  - System I2C Slave: can access system control register, share the ports with I2C0 ports, and work evenly in MCU sleep mode.
  - I2C0 : I2C slave, can be used to program flash memory during booting period.
  - I2C1 : General purpose I2C controller. Master /slave configurable，
  - Chip address configuration: 3 I2C controller has different chip address, you can check the table below.

Table 4-1 I2C address map

I2C_address	I2C0 PORTS		I2C1 PORTS
	System I2C	I2C0 Slave	I2C1 Slave
GPIO_02 Pull Down (during boot stage)	0x2F	0x35	0x35
GPIO_02 no Pull Down(during boot stage)	0x2F	0x36	0x36
Work Status	0x2F	configurable	configurable

- DMA
  - 2 channel DMA
  - Supports 8/16/32/64-bit data width
  - Supports memory-to-memory, memory-to-peripheral, and peripheral-to-memory data transfer types

- UART
  - Integrates 2 UART controllers
  - Full-duplex operation
  - Supports speed up to 1Mbps
  - Supports modem flow control by software or hardware

- SPI Interface
  - Master/slave configurable
  - Polarity and phase of Chip Select and SPI Clock are configurable

- Timer
  - Consists of four 32-bit up-counters

- WDT
  - Programmable and hard coded reset pulse length.
  - An interrupt is generated first, and if the interrupt is not cleared by the service routine before the second timeout, a system reset is generated
  - 32-bit WDT counter

- RTC
  - Alarm function – generates an interrupt after a programmed number of cycles
  - Configurable option to include the prescaler counter.

4.6. Power Management

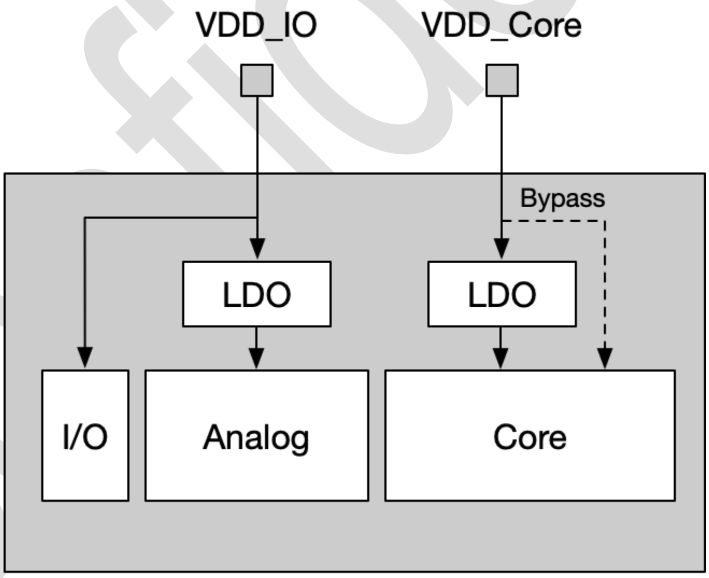


Figure 4-1 Chip power supply system

- I/O voltage support 1.8v/3.3v
- Core voltage support 0.85v~3.3v
- Integrates two LDO for chip power supply. When VDD_Core is lower than 1.0v, the core power LDO will be bypassed.

- Supports DVFS for MCU
- Supports voltage adjustment
- Supports sleep/wake modes. The MCU subsystem can enter into sleep mode and turn the internal power off to reduce power. When voice is detected by VAD or a interrupt is generated by RTC/GPIO, the MCU subsystem can wake up to normal mode.

4.7. Power on and Reset

- Integrates POR(power on reset) module, the power on sequence should meet the following condition:

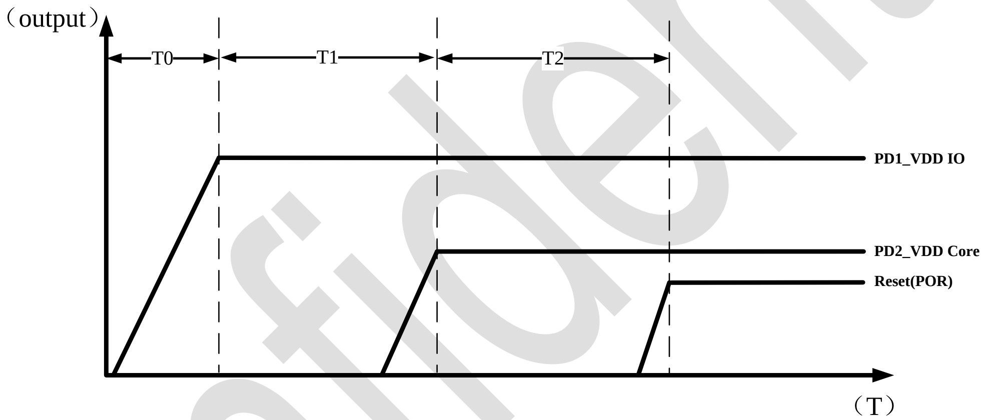


Figure 4-2 Chip power on reset

- T0 < 2ms
- T1: 0~3ms
- T2 > 4 ms

4.8. Audio Interface

4.8.1. Overview

The audio input interfaces of GX8002 include Audio_ADC (built-in), PDM(DMIC interface), I2S, and the audio output interface including two sets of I2S and PWM outs.

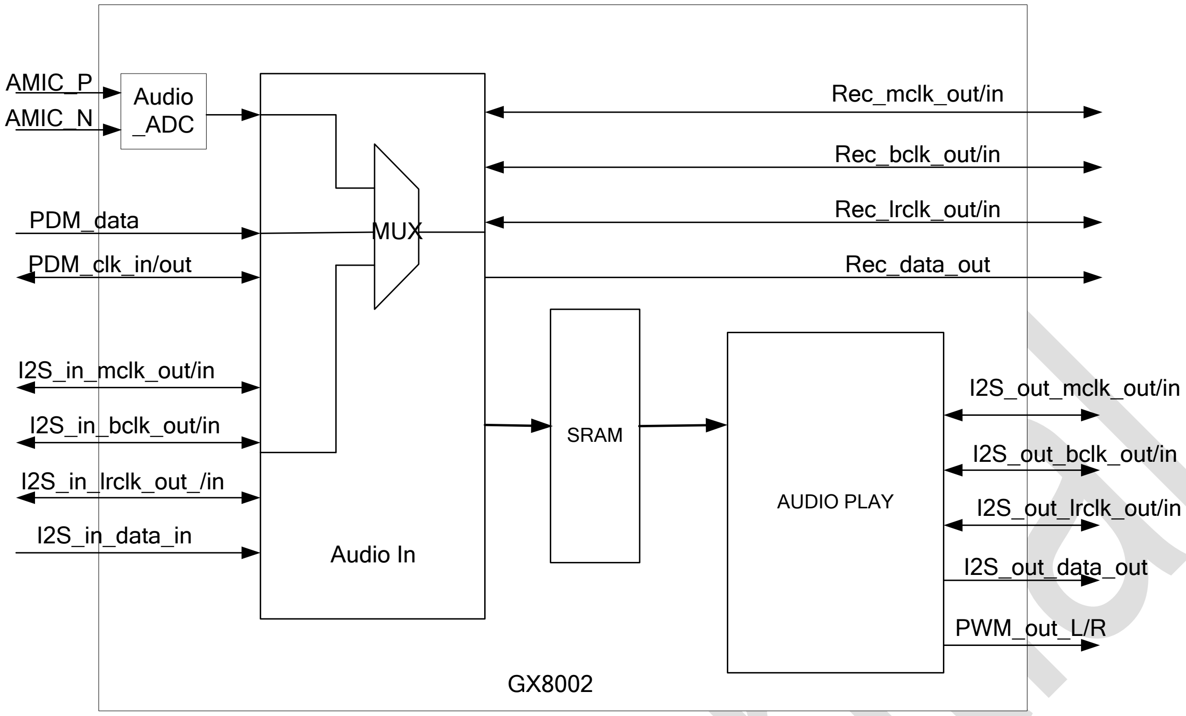


Figure 4-3 Audio I/O interface block diagram

4.8.2.Audio Input Interface

- **Analog Mic Input**
  - Integrates 16-bit 1-channel Audio ADC
  - Sample rate: 16KHz
  - SNR: 65dB

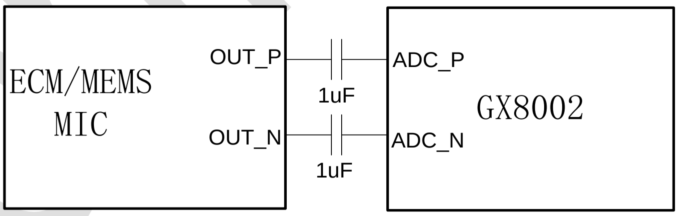


Figure 4-4 Differential AMIC input

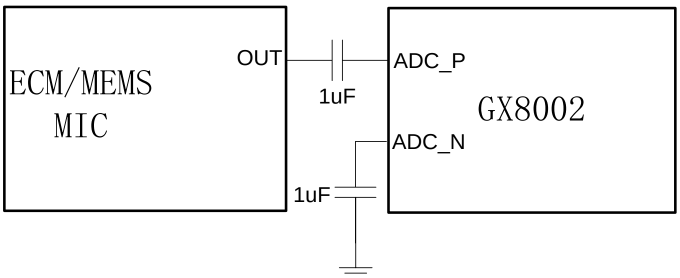


Figure 4-5 Single-ended AMIC input

- **DMIC**
  - Digital microphone(DMIC) supports 1 or 2 channels
  - PDM clk supports master or slave mode.
  - The chip output PDM clk(master mode) is fixed at 1.024MHz, and the external input PDM clk(slave mode) can support 1.024MHz or 2.048MHz.

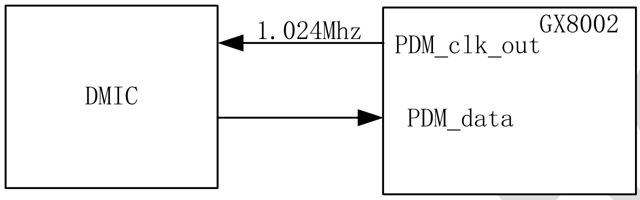


Figure 4-6 Single channel DMIC master mode

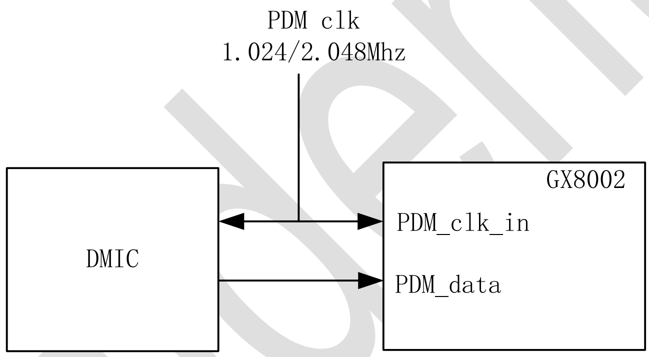


Figure 4-7 single-channel DMIC slave mode

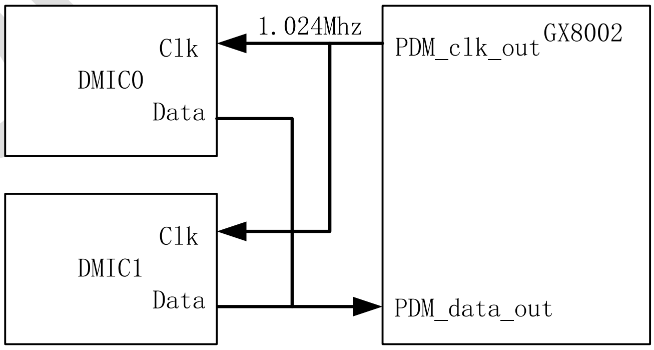


Figure 4-8 2-channel DMIC master mode

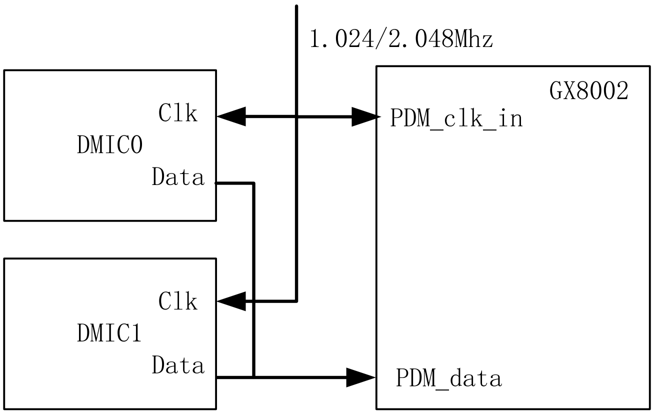


Figure 4-9 2-channel DMIC slave mode

- **I2S IN**
  - I2S IN supports master or slave mode. The chip output mclk(master mode) is fixed at 12.288MHz, and the external input mclk(slave mode) can support 12.288MHz or 24.576MHz.
  - Sample frequency(hereinafter referred to as fs) supports 48KHz、16KHz、8KHz.
  - Bclk supports 32fs、64fs、128fs、256fs, and the latter two are used in TDM mode.
  - Valid pcm data width supports 16 bit、20 bit、24 bit.
  - Data format supports I2S standard mode(including I2S、left justified、right justified) or TDM custom mode(including 64TDM、128TDM、256TDM).
  - Recording and processing support up to 2 channels.

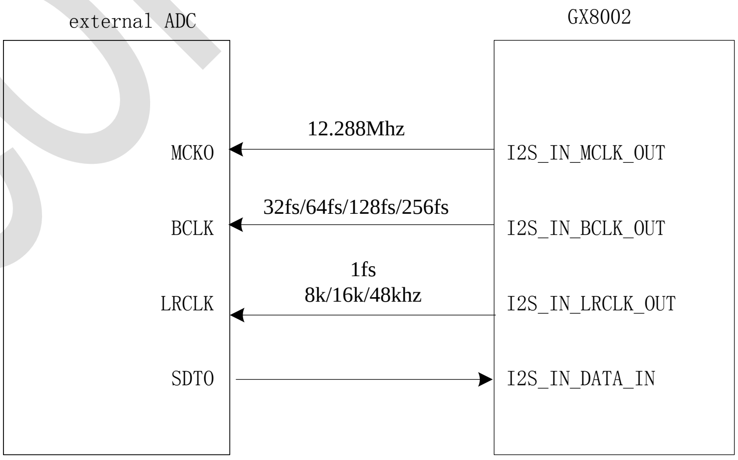


Figure 4-10 I2S IN master mode

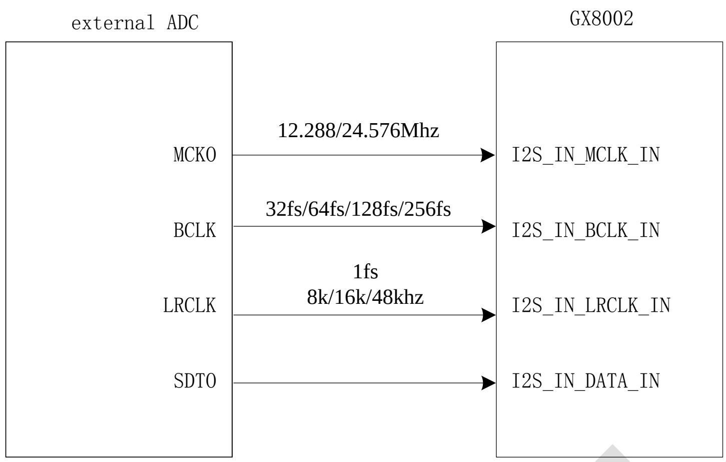


Figure 4-11 I2S IN slave mode

Bclk supports 32fs、64fs in I2S standard mode(including I2S、left justified、right justified). According to the I2S standard, the data changes at the falling edge of the bclk, and collects data at the rising edge of the bclk.

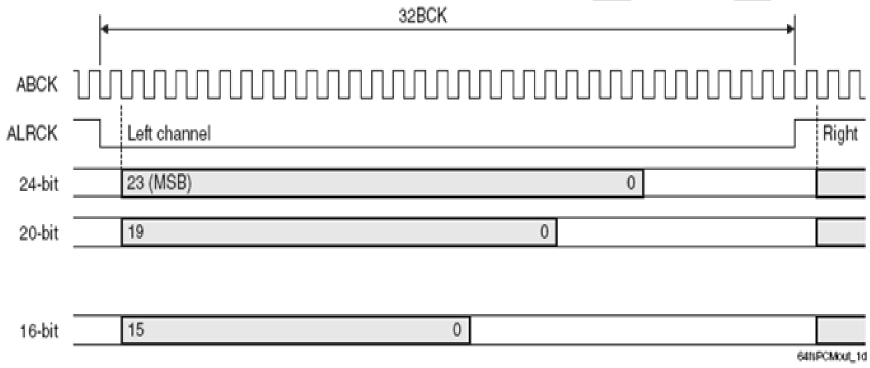


Figure 4-12 I2S data format when bclk=64fs

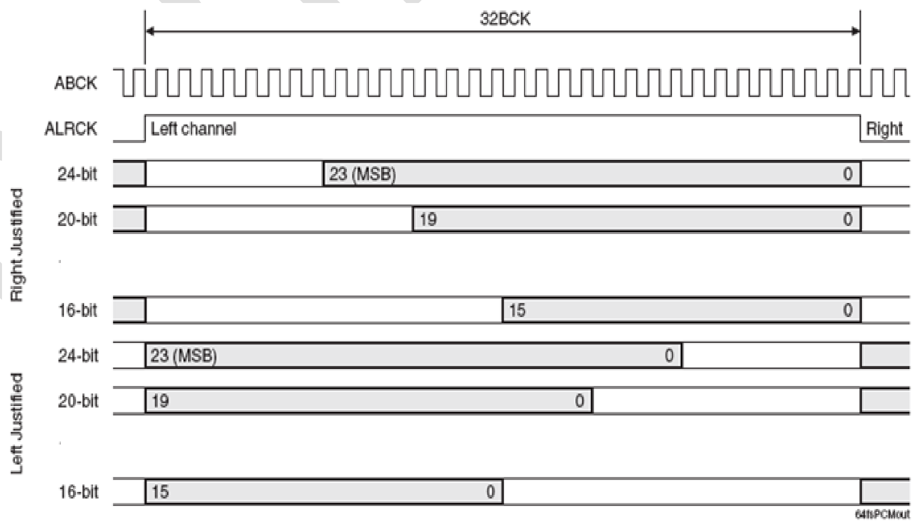


Figure 4-13 Left/right justified data format when bclk=64fs

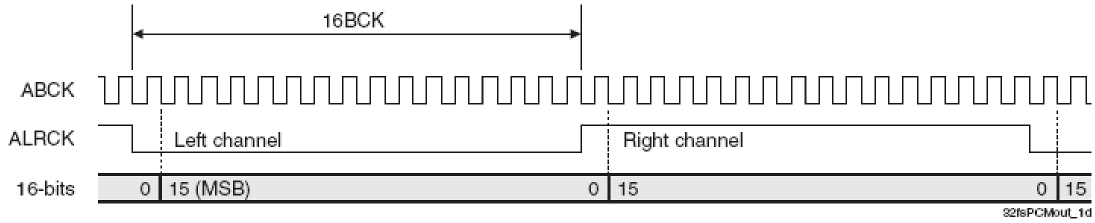


Figure 4-14 I2S data format when bclk=32fs

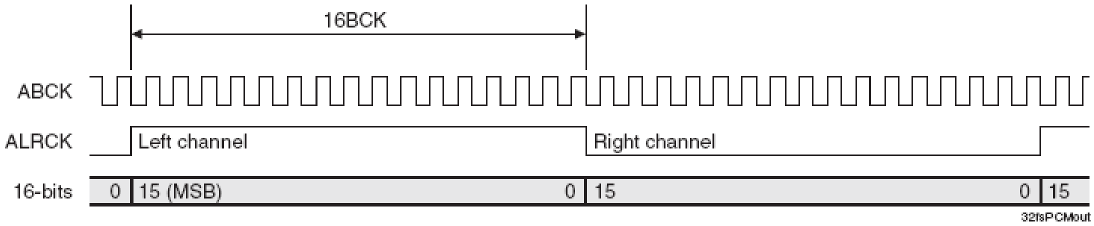


Figure 4-15 Left/right justified data format when bclk=32fs

Because TDM mode(including 64TDM、128TDM、256TDM) is not as standard as I2S standard mode, different manufacturers will have differences. For example, the data may change at the rising or falling edge of the bclk, such as using long frame synchronization mode or short frame synchronization mode. GX8002 supports two long frame synchronization modes and two short frame synchronization modes to meet the above compatibility. The bit width of slot supports 16bit、24 bit、32 bit. Each slot represents the data of one channel. The maximum number of slots is related to the clock of bclk and the bit width of slot.

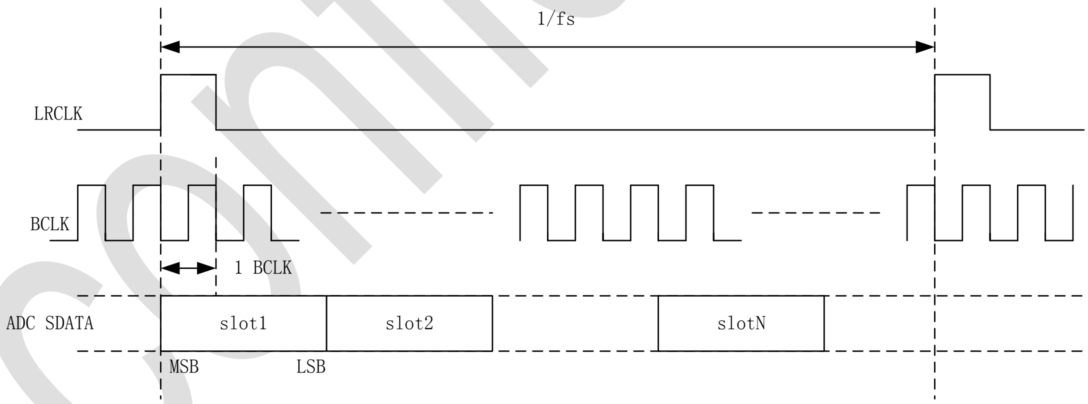


Figure 4-16 Long Frame Sync TDM mode case 0

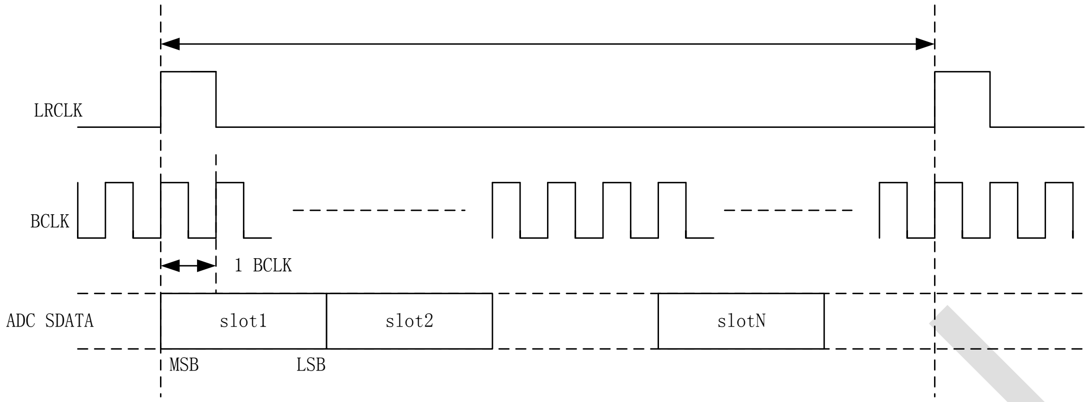


Figure 4-17 Long Frame Sync TDM mode case 1

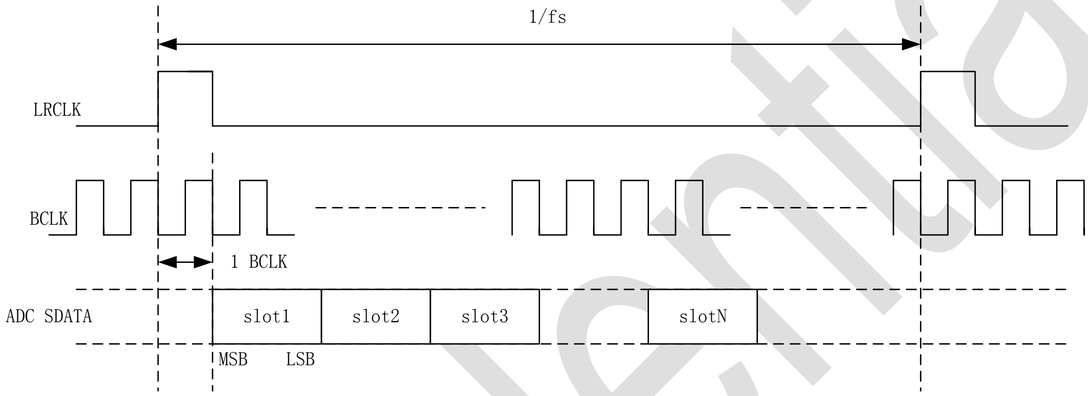


Figure 4-18 Short Frame Sync TDM mode case 0

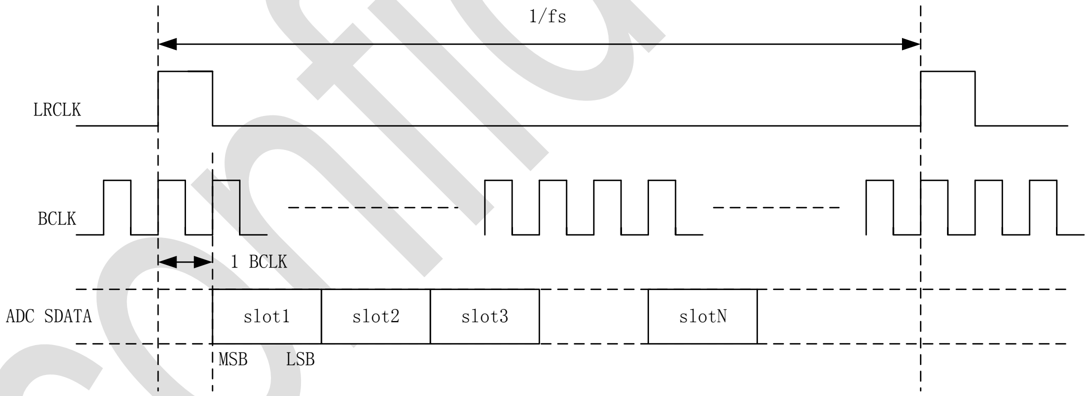


Figure 4-19 Short Frame Sync TDM mode case 1

Table 4-2 Configuration of clock flip registers

Application mode	Bclk_o_inv_en	Lrclk_i_inv_en	Bclk_i_inv_en
TDM long frame case 0 master	set 0	set 0	set 0
TDM long frame case 1 master	set 1	set 0	set 1
TDM short frame case 0 master	set 0	set 0	set 0

Application mode	Bclk_o_inv_en	Lrclk_i_inv_en	Bclk_i_inv_en
TDM short frame case 1 master	set 1	set 0	set 1
TDM long frame case 0 slave	It's ok to set 0 or 1	set 0	set 0
TDM long frame case 1 slave	It's ok to set 0 or 1	set 0	set 1
TDM short frame case 0 slave	It's ok to set 0 or 1	set 0	set 0
TDM short frame case 1 slave	It's ok to set 0 or 1	set 0	set 1
I2S standard mode	set 0	set 0	set 0

Table 4-3 Mclk and TDM mode

Mclk	fs	64TDM (satisfy bclk=64fs)	128TDM(satisfy bclk=128fs)	256TDM(satisfy bclk=256fs)
12.288MHz	16KHz	supported	supported	supported
	8KHz	supported	supported	supported
	48KHz	supported	supported	unsupported
24.576MHz	16KHz	supported	supported	supported
	8KHz	supported	supported	supported
	48KHz	supported	supported	supported

4.8.3.Audio Output Interface

- **Record PCM OUT**
  - Record PCM out ports can output the audio data directly from the audio input channels not from the system SRAM.
  - Record PCM output also use I2S signals and supports master or slave mode. The chip output mclk(master mode) is fixed at 12.288MHz, and the external input mclk(slave mode) can support 12.288MHz or 24.576MHz.
  - Sample frequency(hereinafter referred to as fs) supports 48KHz、16KHz、8KHz.
  - Bclk supports 32fs、64fs.
  - Valid pcm data width supports 16bit、20 bit、24 bit.
  - Data format supports I2S standard mode(including I2S、left justified、right justified).

– Independent selection of content sources of left and right channels, such as AMIC / DMIC0 / DMIC1/ I2SIN0/ I2SIN1 .

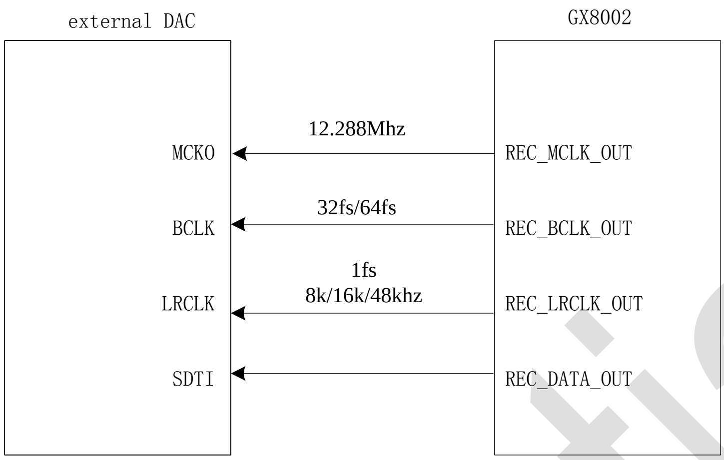


Figure 4-20 Record PCM master mode

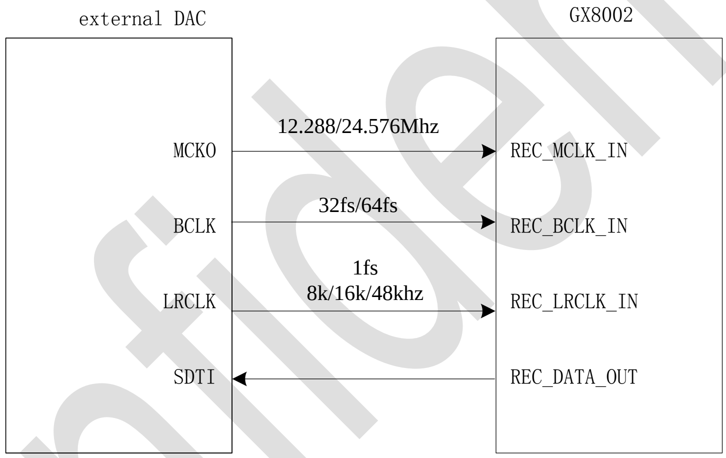


Figure 4-21 Record PCM slave mode

- **I2S OUT**
  – I2S out interface output audio data from the internal audio play module.
  – I2S out supports master or slave mode. The mclk supports 128/256/512/1024fs.
  – Fs supports 8KHz、11.025KHz、16KHz、22.05KHz、24KHz、32KHz、44.1KHz、48KHz.
  – Bclk supports 32fs、64fs.
  – Valid pcm data width supports 16 bit、20 bit、24 bit.

– Data format supports I2S standard mode(including I2S、left justified、right justified).

– Supports volume adjusting.

- **Audio DAC(PWM OUT)**

  – Dual 16-bit DAC PWM output

4.8.4.I2S Five-wire Modes

Two sets of I2S can share MCLK, BCLK and LRCLK in five-wire mode.

- **Five-wire modes summary**

Table 4-4 Five-wire modes

Five-wire modes	GX8002			External Input	External Output
	I2S IN	I2S OUT	I2S REC OUT	(ADC for example)	(DAC for example)
	Master	Slave		Slave	Slave
Master Modes	Master		Slave	Slave	Slave
	Slave	Master		Slave	Slave
Master Modes		Master	Slave		Slave
		Slave	Master		Slave
	Slave	Slave		Master	Slave
	Slave	Slave		Slave	Master
Slave Modes	Slave		Slave	Master	Slave
	Slave		Slave	Slave	Master
		Slave	Slave		Master

- **I2S IN & I2S OUT**

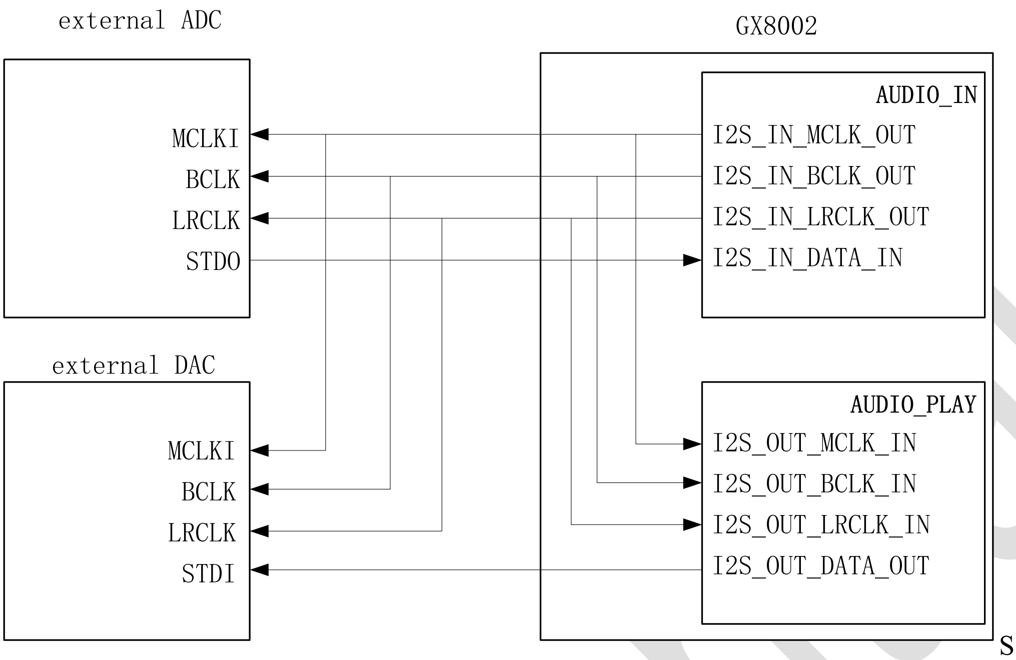


Figure 4-22 Five-wire master mode with I2S_in using master mode and I2S_out using slave mode

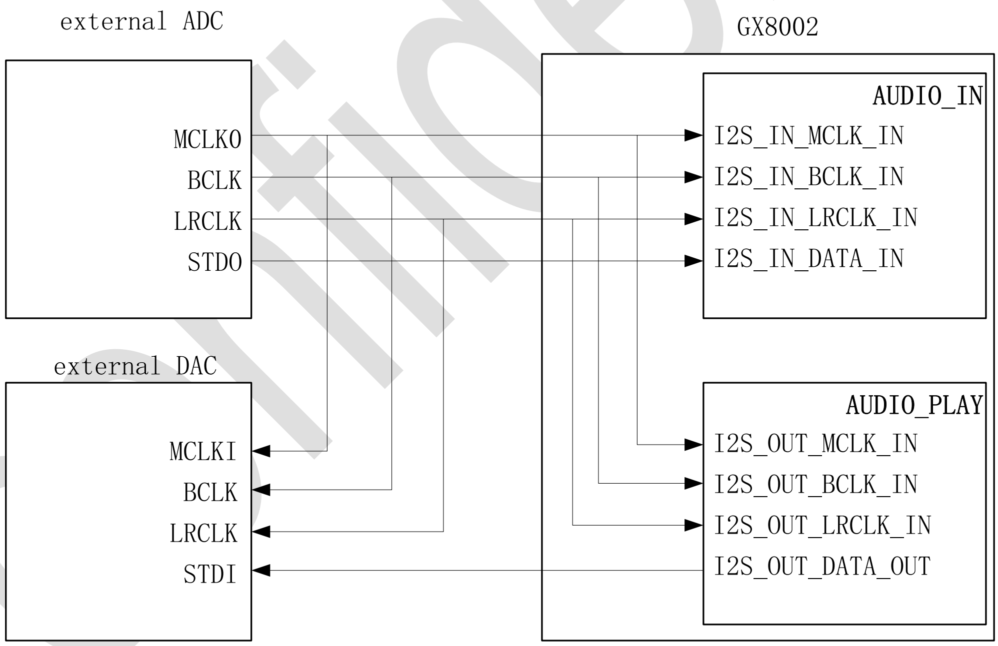


Figure 4-23 Five-wire slave mode with I2S_in and I2S_out using slave mode and external ADC using master mode

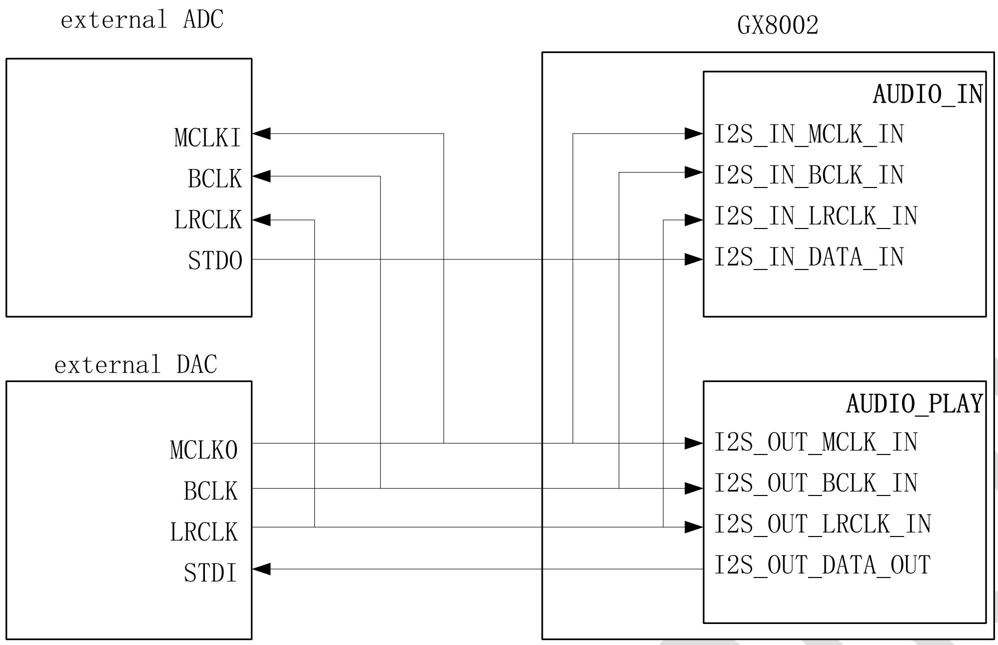


Figure 4-24 Five-wire slave mode with I2S_in and I2S_out using slave mode and external DAC using master mode

4.8.5.Voice Active Detector

- Integrates hardware VAD(Voice Activity Detection)
- Detects human voice by voice spectrum features
- VAD can wake up system from sleep mode

5. Applications

5.1. Smart Earphone

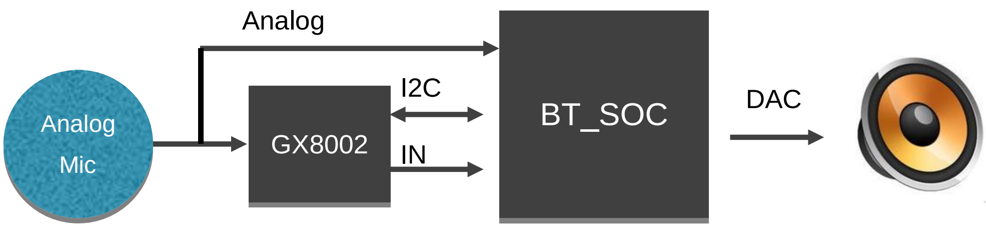


Figure 5-1 Analog microphone connection

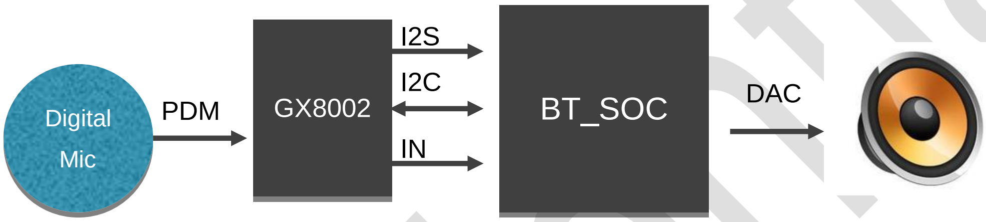


Figure 5-2 Digital PDM microphone connection by master mode

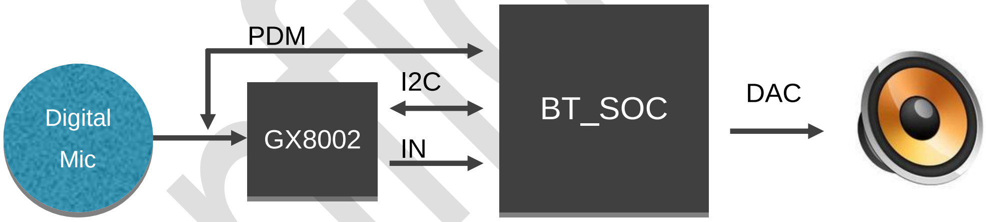


Figure 5-3 Digital PDM microphone connection by slave mode

Key Features:

- Supports PDM and analog type microphone
- Supports voice wakeup, and short commands
- Integrates hardware VAD

5.2. IoT Device Voice Controller

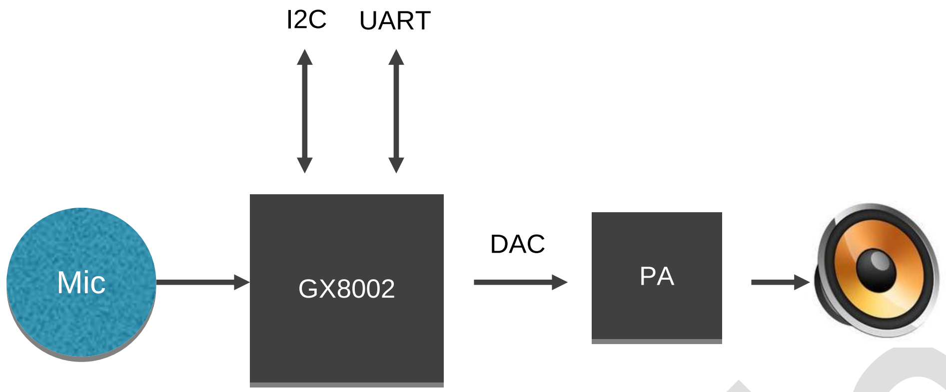


Figure 5-4 GX8002 IoT voice controller application

Key Features:

- Supports PDM and analog type microphone
- Supports voice wake-up, and short commands
- Integrates hardware VAD

6. Electronic Specification

6.1. Recommended Operating Condition for 3.3V IO Application

Table 6-1 Recommended operating conditions for 3.3V IO

Parameters	Min	Typ	Max	Units
IO Power Supply Voltage(VDD_IO)	2.97	3.3	3.6	V
IO Power Supply Current	30	200	500	uA
Output High Level (VOH)	2.4			V
Output Low Level (VOL)			0.4	V
Input High Level (VIH)	2.0		VDD_IO +0.3V	V
Input Low Level (VIL)	-0.3		0.8	V
Input Leakage Current			±10	uA
Pull-up Resistor	27K	40K	65K	Ω

6.2. Recommended Operating Condition for 1.8V IO Application

Table 6-2 Recommended operating conditions for 1.8V IO

Parameters	Min	Typ	Max	Units
IO Power Supply Voltage(VDD_IO)	1.62	1.8	1.98	V
IO Power Supply Current	10	50	300	uA
Output High Level (VOH)	VDD_IO -0.45V			V
Output Low Level (VOL)			0.45	V

Parameters	Min	Typ	Max	Units
Input High Level (VIH)	0.65*VDD_IO		VDD_IO +0.3V	V
Input Low Level (VIL)	-0.3		0.35* VDD_IO	V
Input Leakage Current			±10	uA
Pull-up Resistor	53K	90K	167K	Ω

6.3. Recommended Operating Condition

Table 6-3 Recommended operating conditions

Parameters	Min	Typ	Max	Units
Core Power Supply Voltage*	0.85	1.2	3.6	V
Core Power Supply Current	200	500	1000	uA
Storage Temperature	-40		120	℃
Operating Ambient Temperature	-40		85	℃
Junction Temperature	0		125	℃

*Note: In auto switch mode, when core power is below 1.0v the internal LDO is bypassed and switch to the input power directly, so please avoid to use the external supply voltage of 0.95~1.05v in auto switch mode.

6.4. Electrostatic Discharge

Table 6-4 Electrostatic discharge

Parameters	Min	Max	Units
Human Body Model (HBM)	-2	2	kV
Machine Model (MM) J ESD22-A115C	-200	200	V

NationalChip

6.5. ADC&DAC characteristic

Table 6-5 ADC Characteristic

Parameters	Min	Typ	Max
Resolution	/	16bit	/
SNR @ 1khz, PGA=0dB	/	65dB	/
THD @1khz, PGA=0dB	/	-61.8dB	/

Table 6-6 DAC Characteristic

Parameters	Min	Typical	Max
Resolution	/	16bit	/
SNR @1khz, external crystal	/	-80dB	/
THD @1khz, external crystal	/	0.01%	/

6.6. Power consumption

Table 6-7 Typical power consumption data

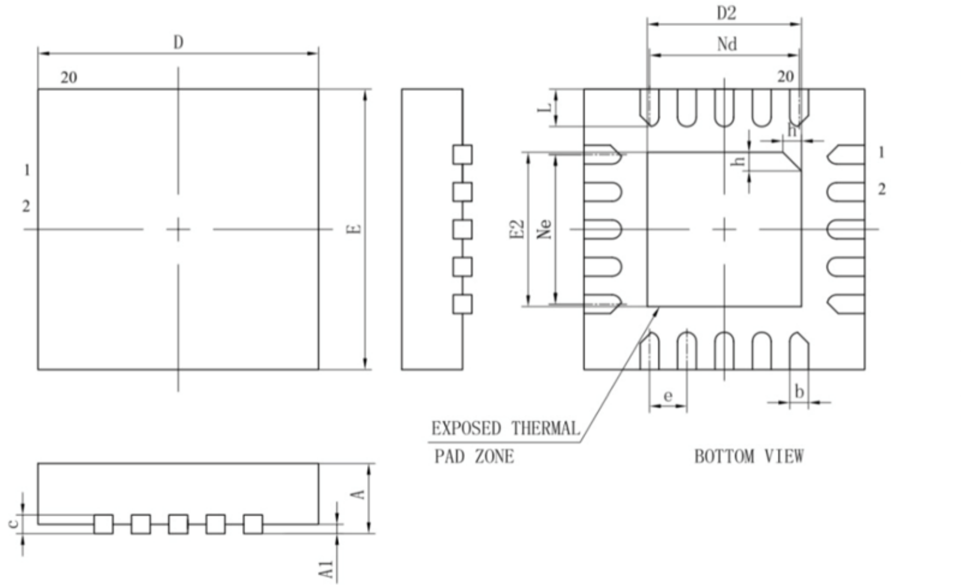
Power supply cases	Supply powers	Standby Current Unit（uA）	Active Current Unit(uA)	Total Power Unit(uW)
Case 0	VDD_IO = 1.8v	7.64	16.76	Standby: 66.6 Active: 467.2
	VDD_Core = 0.85v	62.15	514.16	
Case 1	VDD_IO = 3.0v	9.34	16.55	Standby: 105.5 Active: 690.0
	VDD_Core = 1.2v	64.59	533.64	

Notes:

1. Standby mode: ADC is on, VAD module is working to detect the voice signal.
2. Active mode: ADC, VAD, Audio IN, MCU, NPU and SRAM modules are working to detect the keywords.
3. Power data measured in normal temperature and chip running NationalChip's public SDK and demo KWS model (Only one wake-up word).

7. Package Information

7.1. Package Specification



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 70	0.75	0. 80
A1	—	0. 02	0. 05
b	0. 15	0. 20	0. 25
c	0. 18	0. 20	0. 25
D	2. 90	3. 00	3. 10
D2	1. 55	1. 65	1. 75
e	0. 40BSC		
Ne	1. 60BSC		
Nd	1. 60BSC		
E	2. 90	3. 00	3. 10
E2	1. 55	1. 65	1. 75
L	0. 35	0. 40	0. 45
h	0. 20	0. 25	0. 30
	75*75		

(Note: Dimensions are in millimeters.)

Figure 7-1 QFN20 package specification

7.2. Convection Reflow Profile

The test results meet 3 reflow solderings, and the reflow temperature is 260 degrees. The details are as follows:

Table 7-1 Convection reflow profile

Profile Feature	Note	Pb-Free Assembly
Average ramp-up rate	Tsmax to Tp	0.6~1.5℃/sec
Preheat	-Temperature Min(Tsmin)	150℃
	-Temperature Max(Tsmax)	200℃
	-Time(min to max)(ts)	60-120sec
Time maintained above:	-Temperature(TL)	217℃
	-Time(tL)	60-150 sec

Profile Feature	Note	Pb-Free Assembly
Peak Temperature(Tp)		260℃
Time within 5℃ of actual Peak Temperature(tp)		≥30sec
Ramp-down Rate		≤6℃/ sec
Time 25℃ to Peak Temperature		≤8 min

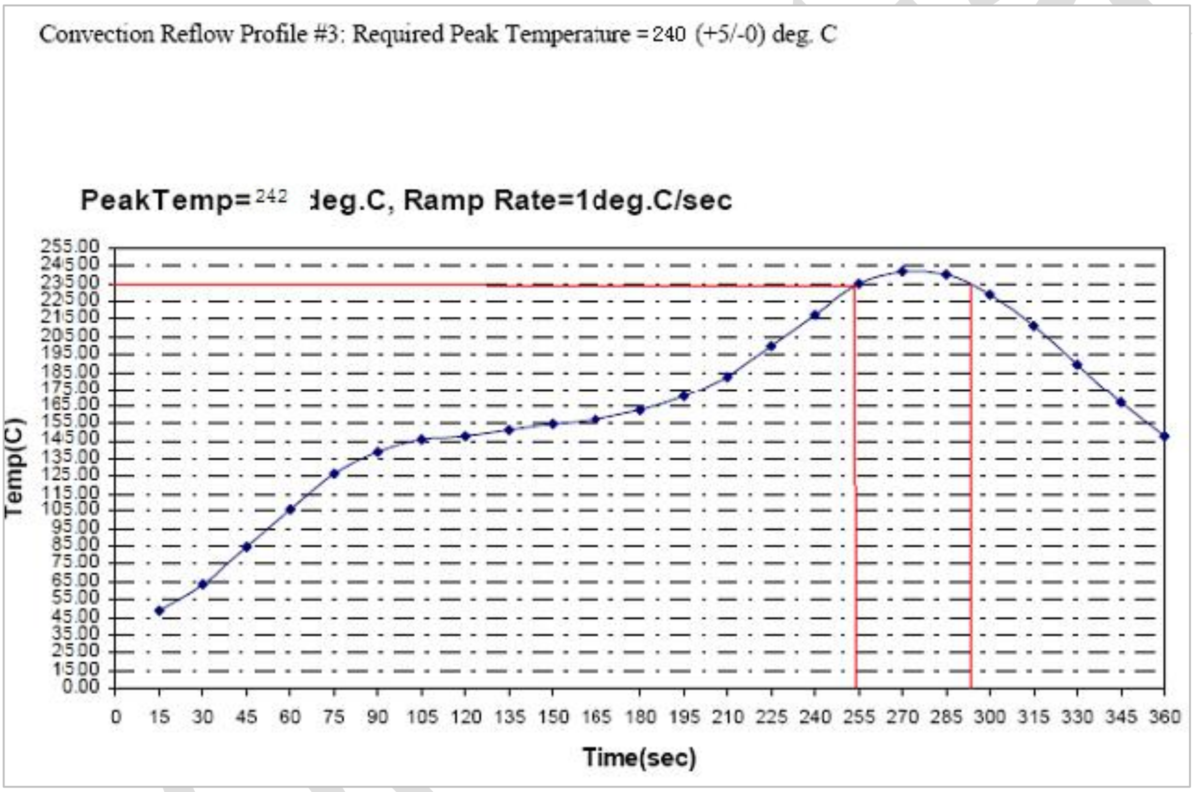


Figure 7-2 Convection reflow profile

8. Ordering Information

Table 8-1 GX8002 ordering information

Ordering Code	Embedded SPI Nor Flash	Package
GX8002A	256KB	QFN20
GX8002B	512KB	QFN20